AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Claim 1. (Currently amended) A ~~carry/majority~~ circuit for arithmetic processing, comprising:

a carry/majority circuit comprising

_____a plurality of differential transistor pairs coupled in parallel with each pair coupled on a first output end of said differential transistor pairs forming a respective leg and a second output end of said differential transistor pairs forming a pair of output nodes, wherein said differential transistor pairs have a single parallel gated level; and

_____a pair of resistors coupled in parallel with a first end coupled to said differential transistor pairs at said respective output nodes; and

a buffer circuit coupled to said output nodes to provide a full differential between said output nodes regardless of inputs to said differential transistor pairs, wherein said buffer circuit is coupled to a clock;

wherein current is steered through said leg of said differential transistor pairs having a higher input voltage.

Claim 2. (Currently amended) The ~~carry~~ circuit according to claim 1, wherein a second end of said resistors are coupled to a ground and each said leg is coupled to a negative voltage supply.

Claim 3. (Currently amended) The ~~carry~~ circuit according to claim 1, wherein a second end of said resistors are coupled to a positive voltage supply and each said leg is coupled to a ground.

Claim 4. (Currently amended) The ~~carry~~ circuit according to claim 1, wherein each transistor of said differential transistor pairs is selected from the group consisting of: bipolar transistors, field effect transistors, metal oxide semiconductor field effect transistors, and insulated gate bipolar transistors.

Claim 5. (Currently amended) The ~~carry~~ circuit according to claim 1, wherein said pair of resistors are matched.

Claim 6. (Currently amended) The ~~carry~~ circuit according to claim 1, wherein a full differential between said output nodes occurs when all inputs or no inputs of said differential transistor pairs are a logic high.

Claims 7 - 8. (Canceled)

Claim 9. (Currently amended) The ~~carry~~ circuit according to claim 1, wherein a voltage level of said output nodes is calculated as the sum of said current multiplied by a resistance value of said resistor.

Claims 10 - 20. (Canceled)